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Date 11-19-02 Serial # 10/010,232 Priority Application Date 12/7/01

Your Name M. Lewis Examiner # _____

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Shelia Clark

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Searcher: 606051826 Structure (#) _____

Searcher Phone: 606051826 Bibliographic ☒

Searcher Location: STIC-EIC2800, CP4-9C18 Litigation _____

Date Searcher Picked Up: 11-19-02 Fulltext _____

Date Completed: 11-19-02 Patent Family _____

Searcher Prep/Rev Time: 20 Other CITEM AB

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Set	Items	Description
S1	3853608	SEMI() CONDUCTOR? OR SEMICONDUCTOR? OR WAFER? OR IC OR INTEGRATED() CIRCUIT? OR SILICON(3N) SUBSTRAT? OR DIE? ?
S2	1634190	CAPACIT?
S3	2924531	SURROUND? OR ENCOMPASS? OR FRAM? OR BORDE? OR ENVELOP? OR - ENCLOS? OR ENCIRCL? OR ENCAS?
S4	508	S2(N) S3
S5	78	S4 AND S1
S6	21	S4(10N) S1
S7	21	S6 AND PY<=2001
S8	18	RD (unique items)
S9	2387	S1(N) S3
S10	83	S9 AND S2
S11	14	S9(10N) S2
S12	14	RD (unique items)
S13	13	S12 NOT S8

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File 2:INSPEC 1969-2002/Nov W3
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File 8:Ei Compendex(R) 1970-2002/Nov W2
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File 99:Wilson Appl. Sci & Tech Abs 1983-2002/Oct
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File 144:Pascal 1973-2002/Nov W3
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File 305:Analytical Abstracts 1980-2002/Nov W1
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File 315:ChemEng & Biotec Abs 1970-2002/Oct
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File 344:Chinese Patents Abs Aug 1985-2002/Oct
(c) 2002 European Patent Office

File 347:JAPIO Oct 1976-2002/Jul (Updated 021104)
(c) 2002 JPO & JAPIO

File 350:Derwent WPIX 1963-2002/UD,UM &UP=200273
(c) 2002 Thomson Derwent

File 202:Information Science Abs. 1966-2002/Oct 29
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File 233:Internet & Personal Comp. Abs. 1981-2002/Nov
(c) 2002 Info. Today Inc.

File 62:SPIN(R) 1975-2002/Oct W2
(c) 2002 American Institute of Physics

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8/9,K/7 (Item 1 from file: 347)
DIALOG(R) File 347:JAPIO
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03057061 **Image available**
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 02-032561 [JP 2032561 A]
PUBLISHED: February 02, 1990 (19900202)
INVENTOR(s): NAKAMURA MINORU
YASUSHIGE HIROAKI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP
(Japan)
APPL. NO.: 63-182877 [JP 88182877]
FILED: July 22, 1988 (19880722)
INTL CLASS: [5] H01L-027/04
JAPIO CLASS: 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R097 (ELECTRONIC MATERIALS -- Metal Oxide Semiconductors,
MOS)
JOURNAL: Section: E, Section No. 915, Vol. 14, No. 178, Pg. 160, April
10, 1990 (19900410)

ABSTRACT

PURPOSE: To acquire a high precision MIS capacitor by providing a capacity of a structure which is provided with an electrode through a dielectric layer on an impurity region of a semiconductor substrate, by enclosing the impurity region by the capacity, and by forming a second dielectric layer which is arranged between the electrode and a first dielectric layer only on a field insulating layer.

CONSTITUTION: A capacity is provided wherein an electrode 16 is arranged through a first dielectric layer 12 and a second dielectric layer 15 of a silicon nitride film and an ASSG layer on an impurity region 17 of a semiconductor substrate 1 of a semiconductor device. The capacity encloses the impurity region 17, a field insulating film 11 is provided to a surface of the substrate 1, and the first dielectric layer 12 extends onto the insulating film 11 and the impurity region 17. The second dielectric layer 15 is arranged between the electrode 16 and the first dielectric layer 12 only on the insulating film 11, and the first dielectric layer which is provided to the upper section thereof is provided to the impurity region to prevent the capacity from being affected by the second dielectric layer.

...PUBLISHED: 19900202)

ABSTRACT

...a silicon nitride film and an ASSG layer on an impurity region 17 of a semiconductor substrate 1 of a semiconductor device. The capacity encloses the impurity region 17, a field insulating film 11 is provided to a surface of...

8/9,K/13 (Item 4 from file: 350)
DIALOG(R) File 350:Derwent WPIX
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010241287 **Image available**
WPI Acc No: 1995-142542/ 199519
XRPX Acc No: N95-112199

Hardening and shaping of tantalum electrolytic capacitor - by making use of shaping dies installed, surrounding capacitor chip which is then pressed after providing anode stick connection with it

Patent Assignee: ROHM CO LTD (ROHL)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 7066090	A	19950310	JP 93210730	A	19930825	199519 B

Priority Applications (No Type Date): JP 93210730 A 19930825

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
JP 7066090 A 5 H01G-013/00

Abstract (Basic): JP 7066090 A

The method involves usage of a hardening cum shaping device. The device consists of an upper shaping die (13), a lower shaping die (14) and side shaping dies (10) provided with a plunger (12). The piece of capacitor chip element (2) is placed in between the lower and upper shaping dies. The upper shaping die has an unit to insert an anode stick (3) to be connected with the capacitor element. The upper and lower dies are pressed towards each other by means of the plunger. The pushing process performed by the dies results in the hardening and shaping of the electrolytic capacitor element.

ADVANTAGE - Facilitates raising of particle density in capacitor chip, lessens number of rejects during mfr.

Dwg.3/13

Title Terms: HARDEN; SHAPE; TANTALUM; ELECTROLYTIC; CAPACITOR; SHAPE; DIE; INSTALLATION; SURROUND; CAPACITOR; CHIP; PRESS; AFTER; ANODE; STICK; CONNECT

Derwent Class: P64; V01

International Patent Class (Main): H01G-013/00

International Patent Class (Additional): B28B-003/02; H01G-009/00

File Segment: EPI; EngPI

Manual Codes (EPI/S-X): V01-B01G; V01-B01G5A; V01-B01G8A

... by making use of shaping dies installed, surrounding capacitor chip which is then pressed after providing anode stick connection with it

8/9,K/17 (Item 8 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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007112650 **Image available**

WPI Acc No: 1987-112647/ 198716

XRPX Acc No: N90-121580

Semiconductor memory device e.g. DRAM mfg. method - uses number of island regions having two resistor cells within each, separated by isolation layer and cylindrical cell capacitor

Patent Assignee: MATSUSHITA ELEC IND CO LTD (MATU); MATSUSHITA ELEC IND KK (MATU)

Number of Countries: 003 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 62058671	A	19870314	JP 85198076	A	19850906	198716 B
US 4920390	A	19900424	US 88218456	A	19880707	199021
KR 9001836	B	19900324				199106
US 5026658	A	19910625	US 89404447	A	19890908	199128

Priority Applications (No Type Date): JP 85198076 A 19850906; JP 85145568 A 19850702

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
JP 62058671 A 16

Abstract (Basic): US 4920390 A

The semiconductor memory device (DRAM) includes a number of island regions, at least one cell transistor disposed on each island region and a cylindrical capacitor surrounding each island region. The capacity of the cell capacitor incorporated -into a small space can be increased.

The method of fabricating the memory device includes a step of forming a groove having a necessary depth in a semiconductor substrate, depositing a membrane having excellent covering characteristics in the groove, etching by using an etching method having a strong anisotropy in the vertical direction while leaving the deposited membrane on a sidewall, and etching the exposed portion of the semiconductor surface deeper in the groove and forming a capacity element and isolation region by using the deep trench.

ADVANTAGE - Has large capacity cell capacitor realised within small space. Can be easily fabricated. (First major country equivalent to J62058671) (24pp Dwg.No.9/10)

Abstract (Equivalent): US 5026658 A

The semiconductor memory device (DRAM) number of island regions, having at least one cell transistor disposed on each region with a cylindrical **capacitor** **surrounding** each region. Also disclosed is method of fabricating a **semiconductor** memory device which includes a step of forming a groove having a necessary depth in a semiconductor substrate, a step of depositing a membrane excelling in coverage on it, a step of etching by an etching method having a strong anisotropy in the vertical direction while leaving said deposit membrane on sidewall, and a step of etching deeper the exposed portion of the semiconductor surface in the groove and forming capacity element and isolation region by using this deep trench.

ADVANTAGE - Capacity of all capacitor incorporated into small space can be increased. (23pp)

Title Terms: SEMICONDUCTOR; MEMORY; DEVICE; DRAM; MANUFACTURE; METHOD; NUMBER; ISLAND; REGION; TWO; RESISTOR; CELL; SEPARATE; ISOLATE; LAYER; CYLINDER; CELL; CAPACITOR

Derwent Class: U11; U12; U13; U14

International Patent Class (Additional): H01L-021/76; H01L-027/04; H01L-029/78

File Segment: EPI

Manual Codes (EPI/S-X): U11-C05G1; U11-C08A3; U12-C02A1; U13-C04B; U14-A03B4

...Abstract (Equivalent): island regions, having at least one cell transistor disposed on each region with a cylindrical **capacitor** **surrounding** each region. Also disclosed is method of fabricating a **semiconductor** memory device which includes a step of forming a groove having a necessary depth in...

?

13/9,K/6 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014339225 **Image available**
WPI Acc No: 2002-159928/200221
XRPX Acc No: N02-122131

Compaction device for making laminated electronic components such as
lamination capacitor , has frame mounted on lower die , surrounding
workpiece, and horizontal type is placed in the space formed between
upper and lower dies

Patent Assignee: NIKKISO CO LTD (NIKK-N)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2001353599	A	20011225	JP 2000176057	A	20000612	200221 B

Priority Applications (No Type Date): JP 2000176057 A 20000612

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2001353599	A	5	B30B-015/02	

Abstract (Basic): JP 2001353599 A

NOVELTY - Auxiliary frame (22) mounted on a lower die (12)
surrounds a workpiece (10). An upper die (16) having flexible layer
(14) presses the workpiece. Horizontal types (20) are arranged at space
between dies.

USE - Compaction device for making laminated electronic components
such as lamination capacitor.

ADVANTAGE - Pressure can be equally applied and any dripping of
angle of workpiece can be prevented effectively by the auxiliary frames
attached to the workpiece.

DESCRIPTION OF DRAWING(S) - The figure shows the main components of
compaction device.

Workpiece (10)
Lower die (12)
Flexible layer (13)
Upper die (16)
Horizontal type (20)
Auxiliary frame (22)
pp; 5 DwgNo 1/5

Title Terms: COMPACT; DEVICE; LAMINATE; ELECTRONIC; COMPONENT; LAMINATE;
CAPACITOR; FRAME; MOUNT; LOWER; DIE; SURROUND; WORKPIECE; HORIZONTAL;
TYPE; PLACE; SPACE; FORMING; UPPER; LOWER; DIE

Derwent Class: P64; P71; V01

International Patent Class (Main): B30B-015/02

International Patent Class (Additional): B28B-003/00; B28B-011/00;

H01G-004/30

File Segment: EPI; EngPI

Manual Codes (EPI/S-X): V01-B03C3A

Compaction device for making laminated electronic components such as
lamination capacitor , has frame mounted on lower die , surrounding
workpiece, and horizontal type is placed in the space formed between
upper and lower dies

13/9,K/12 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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004218087
WPI Acc No: 1985-044967/198508
XRPX Acc No: N85-033452

Integrated, transistor contg. amplifier circuit - has amplifying
transistor base zone for operational frequency to capacitance integrated
in substrate

Patent Assignee: TELEFUNKEN ELECTRONIC GMBH (TELE)

Inventor: BECKENBACH W; RINDERLE H
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 3326957	A	19850214	DE 3326957	A	19830727	198508 B
JP 60043907	A	19850308	JP 84153289	A	19840725	198516
DE 3326957	C	19860731				198631
US 4639686	A	19870127	US 84629619	A	19840711	198706
KR 9303521	B1	19930501	KR 844476	A	19840727	199421

Priority Applications (No Type Date): DE 3326957 A 19830727

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3326957	A		10		
KR 9303521	B1			H03F-003/195	

Abstract (Basic): DE 3326957 A

The base zone of the amplifier transistor for the operational frequency is coupled to the integrated circuit substrate via an integrated capacitance. The latter is preferably 20 times as large as the transistor base-collector capacitance and is of a high-quality design. It may be formed by a pn-junction between a semiconductor zone and a surrounding region in the semiconductor body.

Several strip-shaped zones may be used to form the **capacitance**, forming pn-junctions with **surrounding semiconductor** regions. The zones are contacted by a comb-shaped electrode. In addition to a substrate terminal, in the vicinity of the capacitance, another terminal may be provided for other parts of the integrated circuit.

USE - For reduction of undesirable oscillations.

0/4

Abstract (Equivalent): DE 3326957 C

The base zone of the amplifier transistor for the operational frequency is coupled to the integrated circuit substrate via an integrated capacitance. The latter is preferably 20 times as large as the transistor base-collector capacitance and is of a high-quality design. It may be formed by a pn-junction between a semiconductor zone and a surrounding region in the semiconductor body.

Several strip-shaped zones may be used to form the **capacitance**, forming pn-junctions with **surrounding semiconductor** regions. The zones are contacted by a comb-shaped electrode. In addition to a substrate terminal, in the vicinity of the capacitance, another terminal may be provided for other parts of the integrated circuit.

USE - For reduction of undesirable oscillations. (10pp Dwg.No.0/4

Abstract (Equivalent): US 4639686 A

The circuit includes an amplifier circuit comprising an amplifier transistor connected in a common base configuration. The circuit is integrated and the base zone of the amplifier transistor, at the operating frequency of the amplifier circuit is connected, i.e. short circuited, by an integrated capacitance to the semiconductor substrate of the integrated circuit.

The capacitance is of such dimensions as to be at least 20 times larger than the base-to-collector capacitance of the amplifier transistor. It is advantageous to use the invention in amplifier circuits operating in the VHF range.

ADVANTAGE - Detrimental effect of parasitic base lead inductance is avoided. (5pp)

Title Terms: INTEGRATE; TRANSISTOR; CONTAIN; AMPLIFY; CIRCUIT; AMPLIFY; TRANSISTOR; BASE; ZONE; OPERATE; FREQUENCY; CAPACITANCE; INTEGRATE; SUBSTRATE

Derwent Class: U12; U13; U24

International Patent Class (Main): H03F-003/195

International Patent Class (Additional): H01L-027/06; H01L-029/72; H03F-001/12; H03F-003/19

File Segment: EPI

Manual Codes (EPI/S-X): U12-C01; U13-B01; U13-D01; U24-A02; U24-A06

...Abstract (Basic): Several strip-shaped zones may be used to form the **capacitance**, forming pn-junctions with **surrounding semiconductor** regions. The zones are contacted by a comb-shaped electrode. In

addition to a substrate...

...Abstract (Equivalent): Several strip-shaped zones may be used to form the capacitance, forming pn-junctions with surrounding semiconductor regions. The zones are contacted by a comb-shaped electrode. In addition to a substrate...

13/9,K/13 (Item 8 from file: 350)

DIALOG(R)File 350:Derwent WPIX

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003095605

WPI Acc No: 1981-K5654D/198141

Modular assembly for electronic watch - has lead frame integrated circuit encapsulated in resin body with trimmer capacitor and battery attached to allow removal or adjustment

Patent Assignee: HITACHI LTD (HITA)

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 2072891	A	19811007				198141 B
GB 2072891	B	19820825				198234

Priority Applications (No Type Date): GB 806521 A 19800327; JP 7772041 A 19770620; JP 7795020 A 19770810; JP 7795021 A 19770810; JP 7795022 A 19770810; JP 77147084 A 19771209; JP 77151762 A 19771219; JP 77151763 A 19771219; JP 77154442 A 19771223

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2072891	A		84		

Abstract (Basic): GB 2072891 A

(+10.8.77(3), 9.12.77, 19.12.77(2), 23.12.77(3), 20.1.78-JP-095020/1/2, 147084, 151762/3, 154442/3, 154480, 004365) (943MB) The electronic watch package is provided with holes or grooves in the block (3) of the package (1) to receive a crystal oscillator (5), a temperature compensating capacitor (6) a trimmer capacitor (7), chip capacitors (8,9) and a lamp (10) from the front side of the package (1). Each of the external terminals is spot welded, soldered or silver pasted to the lead conductor on the exposed surface. A battery (11) is inserted from the rear side of the package to be pressed to the lead conductor for electrical connection.

After mounting a light diffusing plate (12) on the integrated circuit enclosure (2) conductive zebra-connectors (13,14) are mounted on the lead conductor interposed between the enclosure (2) and the block (3) and on these connectors (13,14) is mounted an LCD (15). This LCD is fixed to the package (1) by the use of a mounting frame (16). The frame (16) makes contact with each switch portion to provide the external terminal of the switch, while serving to hold the battery (11).

15

Title Terms: MODULE; ASSEMBLE; ELECTRONIC; WATCH; LEAD; FRAME; INTEGRATE; CIRCUIT; ENCAPSULATE; RESIN; BODY; TRIM; CAPACITOR; BATTERY; ATTACH; ALLOW; REMOVE; ADJUST

Derwent Class: S04; U11

International Patent Class (Additional): G04G-001/00; H01L-023/30

File Segment: EPI

Manual Codes (EPI/S-X): S04-B09; U11-D

... has lead frame integrated circuit encapsulated in resin body with trimmer capacitor and battery attached to allow removal or adjustment

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Set	Items	Description
S1	99955	SEMI() CONDUCTOR? OR SEMICONDUCTOR? OR WAFER? OR IC OR INTE- GRATED() CIRCUIT? OR SILICON(3N) SUBSTRAT? OR DIE? ?
S2	16274	CAPACIT?
S3	7385	SURROUND? OR ENCOMPASS? OR FRAM? OR BORDE? OR ENVELOP? OR - ENCLOS? OR ENCIRCL? OR ENCAS?
S4	10	S1 AND S2 AND S3
S5	38	S2(6N) S3
S6	0	S5 AND S1

? show files

File 315:ChemEng & Biotec Abs 1970-2002/Oct

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